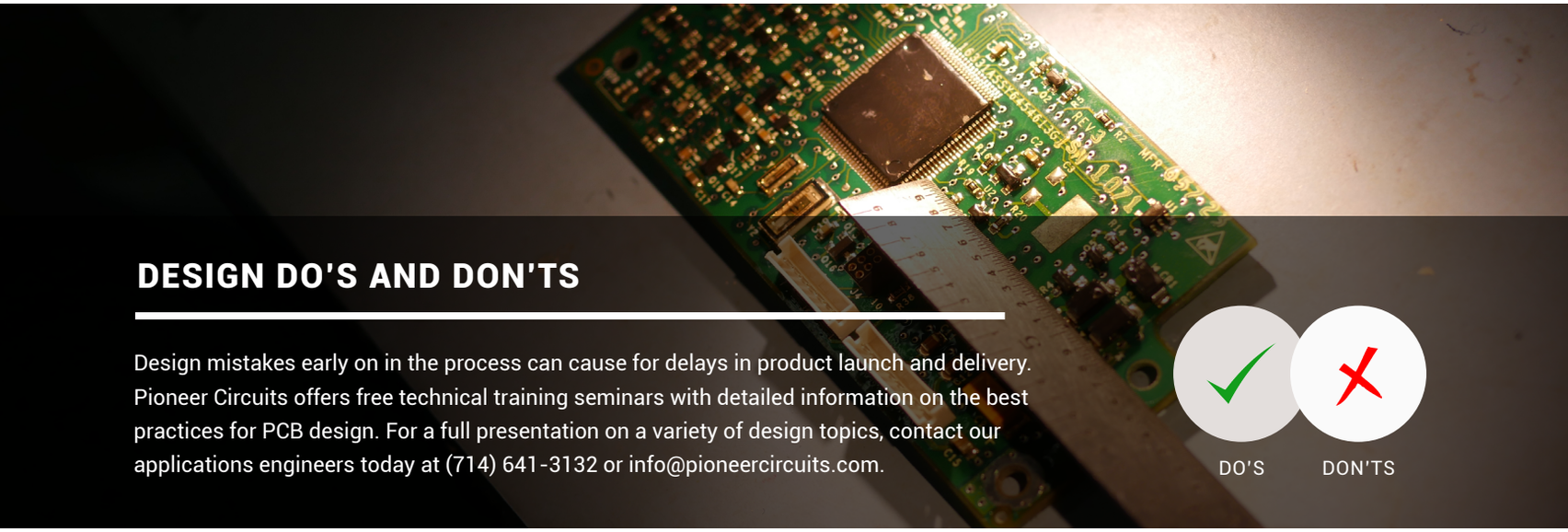
PIONEER CIRCUITS, INC.



DESIGN DO'S AND DON'TS

Design mistakes early on in the process can cause for delays in product launch and delivery. Pioneer Circuits offers free technical training seminars with detailed information on the best practices for PCB design. For a full presentation on a variety of design topics, contact our applications engineers today at (714) 641-3132 or info@pioneercircuits.com.

DO'S DON'TS

1. MOCK-UP SERVICES

Take advantage of mock-up services. Mock-ups help to verify the fit and feel of your design layout and mechanical concept. This ensures that your design will fit correctly into your project without the costs of an actual build.

DO: Use Mock-ups to make sure that your design will fit into your project as planned. Our mock-up services are completely free, providing a no-cost solution to prevent project delays and redesigns.

DON'T: Design a part without checking to make sure that it will fit correctly during final installation. We have had instances where customers had to scrap their part due to lack of planning.

2. DATA & DRAWING MATCH

Data and drawing mismatches can cause major product launch delays. Even the smallest mistakes can be a problem, so be sure to check for things such as drawing to data dimensions, hole quantity, pad size, and revision levels.

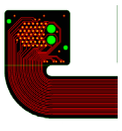
DO: Make sure you are being extra careful with checking that the data and drawings match. We know the largest sources for reported errors and can help with the drawing process to ensure that everything matches.

DON'T: Submit data and drawings without checking hole schedules for correct counts, drawing to data dimensions and radius callouts, notes for line width and spacing requirements back to the original date, and that manufacturing tolerances are taken into consideration.

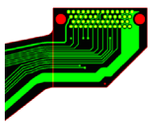
3. STRESS RISERS

Stress Risers are design deficiencies that may cause failures of cracked copper traces. Knowing how to avoid these stress risers is important to avoid project launch delays.

DO: Keep circuit paths perpendicular to the bend, balance construction on each side of the neutral bend axis, and use large radius transitions.



DON'T: Place components or vias in flexible areas or make angular transitions in circuit routings.



4. DESIGN FOR HEAVY COPPER

The impact of line loss (reduction) at etch becomes more challenging at copper weights of 2 oz/ sq ft and above. During the CAM operation, etch loss compensation is added back into the line width to assure the part will meet end product line width requirements.

DO: Make sure that the master artwork has nine to ten mils of available "as-designed" spacing on a two ounce layer.

DON'T: Design without considering the five mil minimum spacing requirement after the etch compensation CAM feature.

www.pioneercircuits.com
3000 S. Shannon St. Santa Ana, CA 92704 | P. (714) 641-3132 | F. (714) 641-3130

5. NON-FUNCTIONAL PADS

Non-functional pads – Who needs them? Not enough real estate to rout that second line between two holes? What if that inner-layer non-functional-pad could go away?

DO: Permit to delete non-functional pads on one side of (heavy) copper layers to create enough room for a second signal. Pioneer Circuits strongly recommends at least .012 distance from a drilled hole barrel (with a removed pad) to any adjacent conductor.

DON'T: Allow no-flow pre-preg to create lack of surface co-planarity due to high "pad stacks". This can be so severe that surface mount devices may not be able to be soldered flat.

6. SURFACE FINISH CONSISTENCY

Selective plating and defining areas of selective surface finish is very important to the design. It is important to make sure that the surfaces on one side of a plated through hole are the same as the opposing side.

DO: Make sure that the same surface that exists on one side of a plated through hole is the same as the other side, and make sure the surface finish on one side is also the same as the other side. We get many designs that do not match, causing a design mess that will lead to delays.

DON'T: Design with nickel/gold finish on one side of a plated through hole and solder on the other. Do not have solder mask coverage or clearance on one side of the plated through hole that is different form the other side or require solder mask on one side only.

7. FORMED FLEX CONFIGURATIONS

Flex layers should be thought of as a rope, not sheet metal. The ability to form or bend a flex-to-install product depends on many different variables, and it is important to understand them.

DO: Make sure to measure in restrained condition, using reference dimensions or specify very large tolerance when designing for formed flex. Flex must be supported by form fixture, especially on the inside of a bend radius.

DON'T: Permit flex to bend in nickel-hole plated areas. Do not design plated through holes in bend regions, and do not use direct force at a flex to rigid transition, for this is a stress riser. Finally, do not hard-dimension or if-dimension.

8. PLATED THROUGH HOLES

The position of plated thorough holes in relation to the flex-rigid transition is a very important part of the design.

DO: Make sure plated through hole barrels are kept at least .100" (.123" preferred) away from the rigid edge to allow correct location of the cover-lay patch termination.

DON'T: Place plated through holes too close to the flex-rigid transition to make sure that the acrylic adhesive of the flex layer cover lay is away from the holes.

9. VIA PROTECTION

Liquid photo-imageable (LPI) solder-mask alone will not "tent" or fill the via hole barrel of solder-mask over bare copper designs, and exposed copper in the barrel could be present.

DO: Protect vias with methods such as applying a thin dry film dot to tent the hole, followed by LPO solder-mask per the design artwork.

DON'T: Design without direction to address via protection. Be sure to refer to your supplier to help with via protection/hole fill options.

10. CONCURRENT ENGINEERING

Concurrent Engineering is a design service that we offer to assist to projects early on in the design stage to make sure that projects run smoothly.

DO: Utilize concurrent engineering to address all of the do's and don'ts mentioned above.

DON'T: Repeat the same mistakes that other engineers have made in the past.

www.pioneercircuits.com
3000 S. Shannon St. Santa Ana, CA 92704 | P. (714) 641-3132 | F. (714) 641-3130